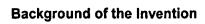
## CACHE CONTROL DEVICE AND METHOD WITH TLB SEARCH BEFORE KEY RECEIP



## Field of the Invention

[0001] The present invention relates to a computer system provided with key control protection by a storage key. More particularly, it relates to a cache control device for controlling the operations of the cache, and a method thereof. Therefor

Description of the Related Art

elated Art a data string used to protect

A storage key is information for protecting the contents of a main storage [0002] of an information processing device from an improper access, and the key is created for each page of the main storage. This storage key consists of, for example, an access control bit (four bits), a fetch protection bit, a reference bit, and a change bit.

Figure 1A is a block diagram showing the constitution of a conventional 100031 information processing unit that has a storage key. The information processing unit of Figure 1A includes a CPU (Central Processing Unit) instruction computation unit 31, a CPU memory unit 32, a main storage 33, and a key storage 41. The CPU memory unit 32 includes two caches 34, a control device 35, a main memory access validity detection circuit 36, two TLBs (Translation Lookaside Buffers) 37, two key buffers 38, a DAT (Dynamic Address Translation) 39, and a key access port 40.

[0004] TLB 37 is provided to speed up address translation, and a correspondence <del>relation</del> between a logical address and a physical address is <del>registered or</del> stored in TLB 37. The key buffer 38 is provided to speed up a key access, and a storage key is <del>-registered or</del> stored in the key buffer 38. Here, the key accessing process <del>demands or request, احويانة العربية ال</del> a storage key stored in the key storage 41, thereby obtaining the key. Further, the cache 34 is provided to speed up a main memory access, thereby storing data faster.

[0005] One of the two caches 34 stores instructions as deta, while the other stores operands as-data. Regarding TLBs 37 and key buffers 38, one is used for instructions, while the other is used for operands. DAT 39 transforms an assigned logical address into a physical address.

[0006] The validity detection circuit 36 checks the validity of the main memory access, using a storage key registered in the key buffer 38 and an access key transmitted from